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Patent Claims

1. A CAM (content addressable memory) apparatus having:
  - 5 a first memory device (10) with a word line input (WL) and at least one storage node (12; 13) for storing a first bit of a data word;
  - 10 a second memory device (11) with a word line input (WL) and at least one storage node (14; 15) for storing a second bit of a data word; and
  - 15 a comparator device (16) for comparing the first and second stored bits with two precoded comparison bits fed via four inputs (20; 21; 22; 23) and for driving a hit node (17) in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit.
- 20 2. CAM apparatus according to Claim 1, characterized in that the comparator device (16) has four signal paths via in each case three transistors (P; N) between a supply voltage ( $V_v$ ) and the hit node (17).
- 30 3. CAM apparatus according to Claim 2, characterized in that the comparator device (16) has a series-parallel circuit comprising twelve field-effect transistors (P; N) of a first conduction type.
- 35 4. CAM apparatus according to Claim 3, characterized in that the comparator device (16) has four parallel-connected series circuits comprising in each case three field-effect transistors (P; N) of the first conduction type.

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5. CAM apparatus according to Claim 2,  
characterized  
in that the comparator device (16) has a series-  
parallel circuit comprising eight field-effect  
5 transistors (P; N) of a first conduction type.
6. CAM apparatus according to one of the preceding  
Claims 2 to 5,  
characterized  
10 in that a first, second, third and fourth storage node  
(12; 13; 14; 15) of the memory devices (10; 11) are  
connected to gate terminals of a first and second  
field-effect transistor (P; N) of the first conduction  
type of a respective path of a series-parallel circuit  
15 in such a way that precisely one path can be switched  
through by each of the four bit combinations possible  
from two bits.
7. CAM apparatus according to Claim 6,  
20 characterized  
in that a respective third transistor of one of the  
four paths is connected, on the gate side, in each case  
to one of the four inputs (20, 21, 22, 23) for feeding  
the two precoded comparison bits.  
25
8. CAM apparatus according to one of the preceding  
Claims,  
characterized  
in that the comparator device (16) has a field-effect  
30 transistor (N; P) of a second conduction type with a  
control terminal (18), which differs from the first  
conduction type, and is located between the hit node  
(17) and a reference potential ( $V_M$ ).  
35 9. CAM apparatus according to Claim 8,  
characterized  
in that the field-effect transistor (N; P) of the  
second power [sic] type can be switched through via the

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control terminal (18) if all the comparison lines (20, 21, 22, 23) have a predetermined signal level.

10. CAM apparatus according to one of the preceding  
5 Claims,

characterized

in that the comparator device (16) has four series-connected field-effect transistors (N; P) of a second conduction type, which differs from the first

10 conduction type.

11. CAM apparatus according to Claim 10,  
characterized

15 in that the four field-effect transistors (N; P) of the second conduction type are connected in series with a series-parallel circuit comprising field-effect transistors (P; N) of the first conduction type between the hit node (17) and a reference potential ( $V_M$ ).

20 12. CAM apparatus according to one of the preceding  
Claims 3 to 11,

characterized

25 in that the field-effect transistors (P; N) of the first conduction type form a p channel and the field-effect transistors (N; P) of the second conduction type form an n channel.

13. CAM apparatus according to one of the preceding  
Claims 3 to 11,

30 characterized

in that the field-effect transistors (P; N) of the first conduction type form an n channel and the field-effect transistors (N; P) of the second conduction type form an p channel.

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14. CAM apparatus according to one of the preceding  
Claims,  
characterized

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in that the comparator device (16) has a holding device (30) for maintaining a signal level at the hit node (17).

5 15. CAM apparatus according to Claim 14,  
characterized

in that the holding device has three transistors, of  
which a first and a second form an inverter (I), the  
input of which is connected to the hit node (17), and

10 the output of which is connected to a gate of the third  
transistor (N; P).

16. CAM apparatus according to one of the preceding  
Claims,

15 characterized

in that a circuit which is upstream of the CAM  
apparatus and serves for generating the two precoded  
comparison bits can be operated statically or  
dynamically.

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17. CAM apparatus according to one of the preceding  
Claims,

characterized

in that both a downstream series pass gate hit path and  
25 a wired-Or hit path can be driven via the hit node  
(17).

18. CAM apparatus according to one of the preceding  
Claims,

30 characterized

in that the memory devices (10; 11) are in each case  
constructed identically and in each case have six  
transistors, four of which form two antiparallel  
inverters (I).